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Parallelizing Applications into Smart Memories - Babb, Rinard, Moritz, Lee.. (Correct) by hand makes it more and more difficult to **design**, develop and debug hardware. This paper as a multi-process state machine in synthesizable **Verilog**. With this system, implemented as a set of SUIF the past decade, hardware **design** languages such as **Verilog** and VHDL enabled a dramatic increase in the www.cag.lcs.mit.edu/~barua/papers/smart-mem.ps.Z

<u>Using on-the-Fly Verification Techniques for the...- Jean-Claude Fernandez (1996) (Correct)</u> transition systems. Formal Methods in System **Design**, 1:251-273, 1992. Kluwer Academic Publishers. partially supported by an industrial contract with **Verilog** in a study for the french DGA (Direction automatique de s'equences de test 11 from **Verilog** as an SDL [3] front-end which produces state ftp.inrialpes.fr/pub/INRIA/projets/VASY/publications/cadp/Fernandez-Jard-Jeron-et-al-96-a.ps.Z

<u>Bisimulation Minimization in an Automata-Theoretic... - Kathi Fisler (1998) (Correct) (2 citations)</u> the required BDDs are prohibitively large for most **designs**. We revisit bisimulation minimization, this time www.cs.rice.edu/~kfisler/Pubs/fmcad98.ps.gz

The START-VOYAGER Parallel System - Ang (1998) (Correct) (1 citation) a novel protection scheme which improves upon past **designs** by not requiring strictly synchronized Performance predictions based on synthesized **Verilog** code show START-VOYAGER's novel message passing derived from simulation with synthesizable **Verilog** code (Section 5)2. Requirements Our basic csg-ftp.lcs.mit.edu/pub/papers/csgmemo/memo-416.ps.gz

The Synchronous System Description Language PURR - Kropf, Ruf, Schneider, Wild (1998) (Correct) of Computer Science, Institute for Computer **Design** and Fault Tolerance (Prof. D. Schmid)P.O. Box description languages such as VHDL [10] or **Verilog** [16]Both languages are dedicated to the to hardware description languages like VHDL or **Verilog**, these languages have been **design**ed with the goethe.ira.uka.de/~schneider/my\_papers/KRSW98a.ps.gz

SpecSyn: An Environment Supporting the... - Gajski, Vahid.. (1998) (Correct) (2 citations)
Paradigm for Hardware/Software System **Design** Daniel D. Gajski, Frank Vahid, Sanjiv Narayan www.cs.ucr.edu/~vahid/courses/269 f98/specsyn tvlsi97.ps

Reversible Computing for Energy Efficient and Trustable.. - Knight, Jr. (1995) (Correct) transactional issues, and programming language **design** which also make fully reversible computer architecture (year 1)ffl MIT will develop full **Verilog** simulations for the reversible architecture, circuits (years 1-2)ffl MIT will develop **Verilog** simulations of a dynamically reconfigurable www.ai.mit.edu/people/cvieri/proposal.ps

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PAM-Blox: High Performance FPGA **Design** for Adaptive Computing Oskar Mencer, Martin
arith.stanford.edu/oskar/fccm98.ps

Statechart Methodology for the Design, Validation, and...- Kol, Ginosar, Samuel (1996) (Correct) (1 citation) Statechart Methodology for the **Design**, Validation, and Synthesis of Large Scale C or Ada) or a hardware description (in VHDL or **Verilog**, at either the behavioral or RTL levels)The compiles the specification into either VHDL or **Verilog**. It can compile into either behavioral or RTL ftp.technion.ac.il/pub/supported/ee/VLSI/async-statecharts.ps.gz

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Design Space Exploration for The Beamformer System - Smita Bakshi Daniel (1993) (Correct) (1 citation) In order to do so, we first define a **parameterized design** template for the beamformer and for a FIR we start by defining and illustrating a **parameterized design** template using several simple examples. recluse.ics.uci.edu/pub/cad/public\_ftp/cadlab-trs/1993/TR-93-34.beamformer\_exploration.ps.gz

Instruction-Processing Optimization Techniques For VLSI.. - Bunda (1993) (Correct) (1 citation) these decisions. Within the framework of a **parameterized design** for a RISC instruction processor, ftp.cs.utexas.edu/pub/techreports/tr93-19.ps.Z

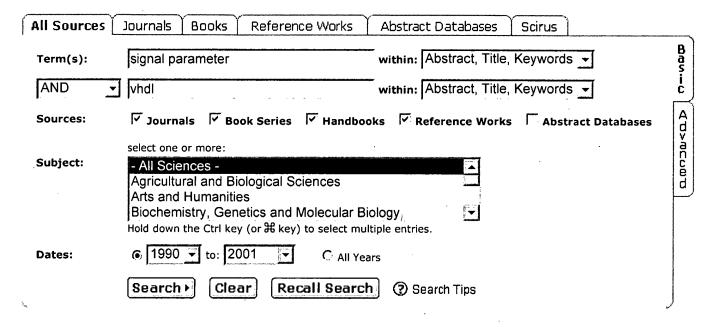
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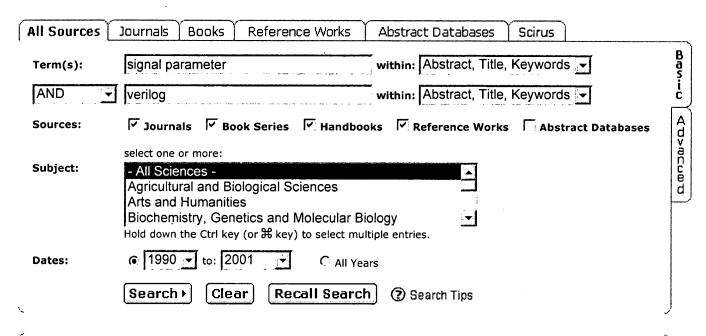
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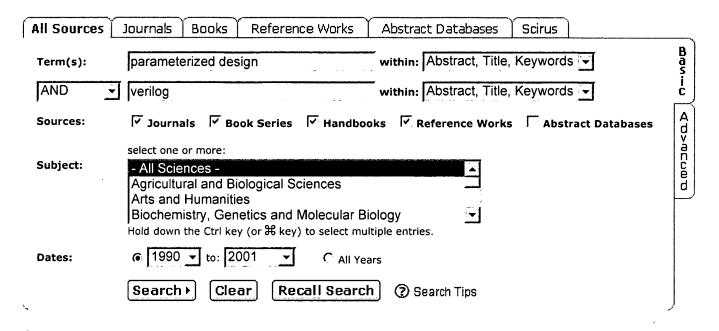
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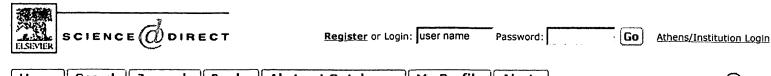


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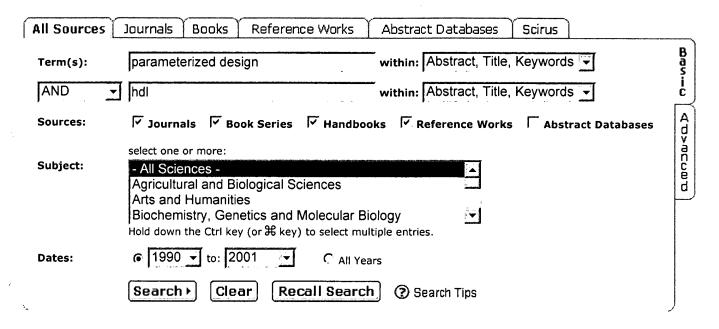
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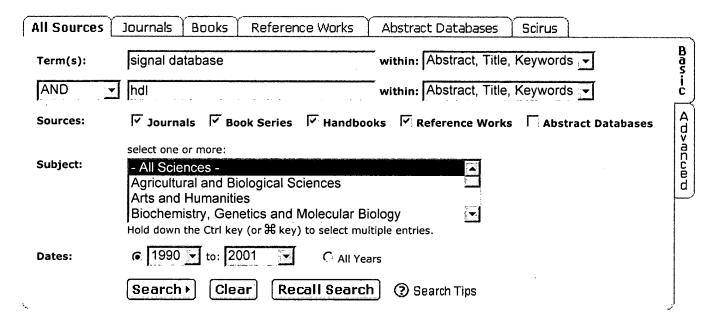
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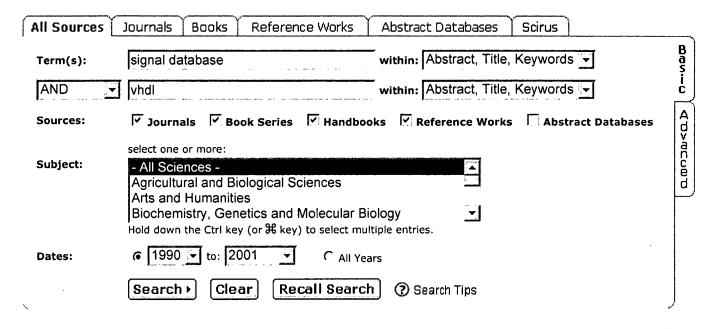
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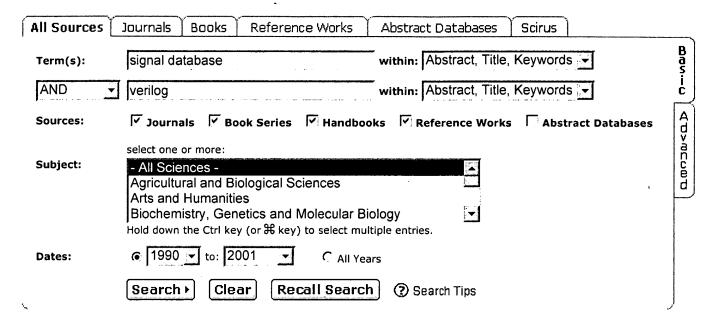
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DC Hyde - Computer Science Department of Bucknell University, Aug. 1997 - karmak.org

... scope(<name>); The <name> parameter must be ... Singh, Y. Trivedi, R. Madhaven and W.

Stapleton, Digital Design and Synthesis with Verilog HDL, published ...

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develop a. **parameterized Verilog** Framework. This is shown in figure 2. ... www.engr.sjsu.edu/electrical/master\_proposal\_example.pdf - Similar pages

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of any parameters until all of the Verilog input files have. been read, because the last file

read might change every. single parameter in the design! ...

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change any parameter on any module. Translation - when compiling a Verilog design,

none of the. parameters in any module are fixed until the last Verilog ...

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#### Creating Verilog HDL Designs for Use with MAX+PLUS II Software

Instantiate any MAX+PLUS II-supported logic function in your **Verilog** HDL **design**. You can enter the following functions:. **Parameterized** and non-**parameterized** ... www.altera.com/support/software/eda\_maxplus2/synplty/vlog/creatv.html - 27k - Cached - Similar pages

### **Verilog HDL: Parameterized Counter**

Altera offers users design examples for use in designs for Altera devices. ... Verilog HDL:

Parameterized Counter. This example shows how to instantiate an ...

www.altera.com/support/examples/verilog/ver\_check\_lpm.html - 22k -

Cached - Similar pages

#### SOCcentral: New Verilog-2001 Techniques for Creating Parmeterized ...

With respect to coding parameterized Verilog models, two Verilog constructs that are ...

Access the entire document on the Sunburst Design, Inc. website. ...

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## SoftJin Technologies :: Enabling Electronic Design

Compliant with IEEE 1364 Verilog standard • Supports behavioral, RTL and netlist

description • Supports parameterized design ...

www.softjin.com/html/verilog.htm - 18k - Cached - Similar pages

#### IP Configuration Management with Abstract Parameterizations

The main focus of CoMAP is on VHDL and **Verilog** based hardware **design** flows, but its modular **design** enables the integration of any **parameter** related language ... www.us.**design**-reuse.com/articles/article5327.html - 70k - <u>Cached</u> - <u>Similar pages</u>

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programming will be posted this week. 6.375 Spring 2006 • L03 Verilog 2 - Design

Examples • 3. Verilog Design Examples. • Parameterized Static Elaboration ...

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# [воок] Advanced programming in the UNIX environment - group of 5 »

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WR Stevens... - 1992 - yendor.com

... and raise Functions \* alarm and pause Functions \* Signal Sets \* sigprocmask ... Appendix

B. Miscellaneous Source Code Our Header File \* Standard Error Routines. ...

Cited by 392 - Cached - Web Search - Library Search

#### [воок] Introduction to signal processing - group of 4 »

SJ Orfanidis - 1996 - ece.rutgers.edu

... Signal averaging ... generator (interpolation) DFT/FFT Functions bitrev.c - bit reversed

index complex.c - complex arithmetic in C cmplx.h - header file for complex ...

Cited by 222 - Cached - Web Search - Library Search

#### The MIT-BIH Arrhythmia Database on CD-ROM and software for use with it

GB Moody, RG Mark, C MIT - Computers in Cardiology 1990. Proceedings., 1990 - ieeexplore.ieee.org

... Each signal file contains two signals sampled at 360 Hz. 'Header' files include

infor- mation about the leads used, the patient's age, sex, and medi ...

Cited by 65 - Web Search

#### The Koala component model for consumer electronics software - group of 3 »

R van Ommering, F van der Linden, J Kramer, J ... - Computer, 2000 - ieeexplore.ieee.org

... This signal is fed to a high-end input processor (HIP) that produces decoded ... For

each module. Koala generates a header file with renaming macros, as shown in ...

Cited by 188 - Web Search - BL Direct

## AFNI: software for analysis and visualization of functional magnetic resonance neuroimages - group of 8 »

RW Cox - Comput Biomed Res, 1996 - afni.nimh.nih.gov

... in AFNI are organized into "datasets." A dataset is a 3D brick of 16-bit values,

with some associated information stored in a separate header file. ...

Cited by 753 - Web Search - BL Direct

#### [PS] System Level Design Using the SystemC Modeling Platform

J Gerlach, W Rosenstiel - Worshop on System Design Automation SDA, 2000 - www-ti.informatik.uni-tuebingen.de

... 5 shows the corresponding source code file. In the top-level routine, all process

header filesand the ... object, which is a special signal, is instantiated. ...

Cited by 38 - View as HTML - Web Search

#### Development of the polysomnographic database on CD-ROM - group of 5 »

Y Ichimaru, GB Moody - Psychiatry and Clinical Neurosciences, 1999 - Blackwell Synergy

... record has a header file, which contains general information about the record such

as its length, gains and offset of each physiological signal, data structure ...

Cited by 11 - Web Search - BL Direct

# A database for evaluation of algorithms for measurement of QT and other waveform intervals in the ECG - group of 3 »

P Laguna, RG Mark, A Goldberg, GB Moody - Computers in Cardiology 1997, 1997 - ieeexplore.ieee.org

... Each record includes a signal file (record dat, where record is the record name).

a header file (record hea, describing the format of the signal file), and sev ...

Cited by 37 - Web Search - BL Direct

#### A stream input-output system - group of 28 »

DM Ritchie - AT&T Bell Laboratories Technical Journal, 1984 - cm.bell-labs.com

... from input and output queues after a signal or on ... into data blocks starting with

a header giving the ... communicates through the terminal module, a file pair, and ...

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verilog header file

1970

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... This is different to languages like **Verilog** that only ... 5 shows the corresponding source code **file**. In the top-level routine, all process **header** filesand the ...

Cited by 38 - View as HTML - Web Search

### Hardware Object Programming on the EVC1-a Reconfigurable Computer - group of 4 »

S Casselman, M Thornburg, J Schewel - FPGAs for Rapid Board Development and Reconfigurable ..., 1995 - arco.unex.es ... via schematic and VHSIC Hardware Description Language (VHDL) or **Verilog** hardware description ... The rawbits **file** is converted into a .h **header file** by a program ... Cited by 4 - View as HTML - Web Search

## [воок] The Complete Verilog Book

V Sagdeo - 1998 - books.google.com ... one to define text substitutions and to indude **files**, which are defined in ... Synthesis is an essential part of today's design process, and **Verilog** HDL usage for ... Cited by 7 - Web Search - Library Search

## [воок] Principles of Verilog Pli

S Mittra - 1999 - books.google.com
... A PLI ROUTINE 23.1 Step I: Including the **header files** 33.2 Step ... err\_intercept
53.3.4 veriusertfs 3.3.5 pli.tab **file** inVCS environment ... FUNDAMENTALS OF **VERILOG** FL ...
Cited by 8 - Web Search - Library Search

#### The use of SystemC for design verification and integration test ofIP-cores - group of 6 »

A Fin, F Fummi, D Signoretto - ASIC/SOC Conference, 2001. Proceedings. 14th Annual IEEE ..., 2001 - ieeexplore.ieee.org ... view the core interface (the class declaration in the **header file**) and the ... descriptions to very accurate gate-level representations (VHDL or **Verilog**) by using ... Cited by 4 - Web Search

#### Exploiting the Power of Vera: Creating Useful Class Libraries

J Bergeron, D Simmons - Proceedings of Synopsys Users Group, 2000 - vlsidsp.el.yuntech.edu.tw ... In **Verilog**, global variables are the norm, so **Verilog** programmers may have to learn to resist the ... First, one of the **header file** must be generated manually. ... <u>Cited by 2 - View as HTML - Web Search</u>

#### SystemC Overview - group of 2 »

M Ganguly - Synopsys Inc, 2001 - www-cad.eecs.berkeley.edu
... Verilog VHDL Co-sim Interface Verilog VHDL Co-sim Interface Import Export Page 30.
Testbench // Header File #include "systemc.h" SC\_MODULE(adder\_reg\_tb) { ...
Cited by 1 - View as HTML - Web Search

#### "full case parallel case", the Evil Twins of Verilog Synthesis - group of 4 »

CE Cummings - 1999 - sunburst-design.com
... Inferred memory devices in process in routine mux3a line 7 in file '.../mux3a.v ...
recognize two directives when added to the end of a Verilog case header. ...
Cited by 1 - View as HTML - Web Search

#### A Verilog to C compiler - group of 3 »

DJ Greaves - Rapid System Prototyping, 2000. RSP 2000. Proceedings. 11th ..., 2000 - ieeexplore.ieee.org ... The **Verilog** shown in ... in- clude the housekeeping lines generated by the real compiler, which include the inclusion of "ttvinc", other **header files** and so ... <u>Cited by 2 - Web Search</u>

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M Zibulevsky, BA Pearlmutter - Neural Computation, 2001 - neco.mitpress.org ... We tested two methods with these **data**. ... Let us consider finding the sparsest **signal** that can be obtained by a linear combination of the sensor **signals** s=w T X ... Cited by 160 - Web Search - BL Direct

## A self-describing data transfer methodology for ITS applications - group of 8 »

DJ Dailey, DF Meyers - Intelligent Transportation System, 1997. ITSC 97. IEEE ..., 1997 - ieeexplore.ieee.org ... mecha- nism for distributing ITS **data** to Information ... devices such as traffic **signal** controllers, envi ... sensor stations, dynamic message **signs**, highway advisory ... Cited by 13 - Web Search - Library Search - BL Direct

#### A software design method for real-time systems - group of 8 »

H Gomaa - Communications of the ACM, 1984 - portal.acm.org ... to wait for an acknowledgment before Output Axis **Data** can output ... queue, as well as Stop and Resume event **signals** from the ... If so, it waits for a Resume **signal**. ... Cited by 67 - Web Search

#### [воок] Data compression: methods and theory

JA Storer - 1987 - Computer Science Press, Inc. New York, NY, USA ... Dictionaries, Journal of VLSI **Signal** Processing Systems ... Practical prefetching via **data** compression, ACM ... Muthukrishnan, Optimal parallel **dictionary** matching and ... <u>Cited by 245 - Web Search - Library Search</u>

# <u>Building a dictionary for genomes: Identification of presumptive regulatory sites by statistical ...</u> - group of 35 »

HJ Bussemaker, H Li, ED Siggia - Proceedings of the National Academy of Sciences, 2000 - pnas.org ... the fluctuations and thus meaningful **signals** in the ... among all segmentations of the **data**; then the ... **dictionary** does not distinguish between **signal** and background ... <u>Cited by 123</u> - Web Search - BL Direct

# The PROSITE dictionary of sites and patterns in proteins, its current status - group of 7 »

A Bairoch - Nucleic Acids Res, 1993 - pubmedcentral.nih.gov ... The PROSITE dictionary of sites and patterns in proteins, its ... The SWISS-PROT protein sequence data bank ... Staden R. Computer methods to locate signals in nucleic ... Cited by 709 - Web Search - BL Direct

#### Learning pronunciation dictionary from speech data - group of 3 »

CM Westendorf, J Jelitto - Spoken Language, 1996. ICSLP 96. Proceedings., Fourth ..., 1996 - ieeexplore.ieee.org ... the data base are the (unla- beled) signals and their ... which actually occured in the data or which ... a lat- tice of phonemic hypotheses from the speech signal. ... Cited by 8 - Web Search

# ... Evaluation of a **Data** Mining Approach to Aid Finding New Adverse Drug Reaction **Signals** in the WHO ... - group of 4 »

M Lindquist, M Ståhl, A Bate, IR Edwards, RHB ... - Drug Safety, 2000 - ingentaconnect.com ... programme is to identify early **signals** of safety ... It complements the previous **signal** generation procedure which in ... new system is based on a **data** mining technique ... Cited by 32 - Web Search - BL Direct

design signal dictionary

1970

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GGE Gielen, RA Rutenbar - Proceedings of the IEEE, 2000 - ieeexplore.ieee.org
 What is needed to expedite the analog and mixed-signal design process is a structured methodology and supporting CAD tools to manage the entire design process ...
 Cited by 121 - Web Search - BL Direct

Fault dictionary based upon stimulus design

H Schreiber - Circuits and Systems, IEEE Transactions on, 1979 - ieeexplore.ieee.org ... in **signal** space, and the fault **dictionary** is constructed ... allow the dimension of the **signal** space to ... The theory of stimulus **design** for fault isolation in linear ... Cited by 18 - Web Search

Blind Source Separation via Multinode Sparse Representation

M Zibulevsky, YY Żeevi... - Neural Computation, 2001 - citeseer.ist.psu.edu ... related documents): More All 0.3: Excitation Codebook **Design** For - Coding ... separation by sparse decomposition in a **signal dictionary** - Zibulevsky, Pearlmutter ... Cited by 30 - Cached - Web Search - BL Direct

A theory for multiresolution signal decomposition: the wavelet representation - group of 16 »

SG Mallat - Pattern Analysis and Machine Intelligence, IEEE Transactions ..., 1989 - ieeexplore.ieee.org A theory for multiresolution **signal** decomposition: the waveletrepresentation.

Mallat, SG Dept. of Comput. Sci., New York Univ., NY; ...

Cited by 5041 - Web Search - Library Search

**Design** of a linguistic statistical decoder for the recognition of continuous speech

F Jelinek, L Bahl, R Mercer - Information Theory, IEEE Transactions on, 1975 - ieeexplore.ieee.org ... **Design** of a Linguistic Statistical Decoder for ... Although the probabilities for the phonemic **dictionary** and phonological ... deter- mine for an acoustic **signal** A and ... Cited by 60 - Web Search

A design-for-test methodology for active analog filters

M Soma - Test Conference, 1990. Proceedings., International, 1990 - ieeexplore.ieee.org ... Lin and Elcherif [2] studies the analog fault **dictionary** approach with ... for analog macrocircuits frequently used in VLSI and **signal** processor **designs**. ... Cited by 85 - Web Search

Challenges in analog and mixed-signal fault models - group of 2 »

M Soma - Circuits and Devices Magazine, IEEE, 1996 - ieeexplore.ieee.org ... customary with past developments, however, **design** outpaces testing ... critical area of mixed-**signal** testing-and ... Analog circuits fault **dictionary**— new approaches ... Cited by 20 - Web Search - BL Direct

Optimized signal expansions for sparse representation - group of 3 »

SO Aase, JH Husoy, J Skretting, K Engan - ... Acoustics, Speech, and **Signal** Processing, IEEE Transactions ..., 2001 - ieeexplore.ieee.org

... motivates our own algorithm for transform vector **design** is reported ... part, we find approximations to the training **signal** using an ini- tial **dictionary** or the ... <u>Cited by 11 - Web Search - BL Direct</u>

[воок] Adaptive system identification and signal processing algorithms N Kalouptsidis, S Theodoridis - 1993 - Prentice-Hall, Inc. Upper Saddle River, NJ, USA

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1970 - 2001

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NH Lovell, F Magrabi, BG Celler, K Huynh, H ... - Engineering in Medicine and Biology Magazine, IEEE, 2001 - ieeexplore ieee.org

... The relational database facilitates fast schema **design** and easy maintenance. ... lection of a patient table from a set of tables in a biomedical **signals database**. ...

Cited by 22 - Web Search - BL Direct

Relational database: a radiation therapy machine control softwaredevelopment tool

J Jacky, R Risler, S Brossard, I Kalet - Engineering in Medicine and Biology Society, 1989. Images of ..., 1989 - ieeexplore ieee.org

... The **Signals Database** The CNTS control system includes over 1000 digital and ... documents and computer text files, including service manuals, **design** drawings and ... <u>Cited by 1 - Web Search</u>

<u>Database on mRNA-Located Eukaryotic Expression Signals Influencing Translation Efficiency and ...</u> - group of 2 »

AV Kochetov, D Grogorovich, NA Kolchanov, A Sarai - GENOME INFORMATICS SERIES, 2001 - hc.ims.u-tokyo.ac.jp ... Keywords: translational **signals**, **database**, mRNA, enhancer 1 Introduction ... COMMENT **design** of reporter GUS gene mRNA 5'UTR in experiment: first 23 nt were.. ... Cited by 1 - View as HTML - Web Search - BL Direct

An integrated architecture for signal validation in power plants - group of 2 »

BR Upadhyaya, TW Kerlin, KE Holbert, O Glockler, ... - Intelligent Control, 1988. Proceedings., IEEE International ..., 1988 - ieeexplore.ieee.org

... In the **design** of future advanced reactors, such as the advanced liquid ... 4 684 SIGNAL VALIDATION SYSTEM ARCHITECTURE PLANT\_SUBSYS PLANT **SIGNALS DATABASE** t ii It ... Web Search

SUTIL: Intelligent ischemia monitoring system - group of 5 »

J Vila, J Presedo, M Delgado, S Barro, R Ruiz, F ... - INT J MED INF, 1997 - www-gsi.dec.usc.es Page 1. International Journal of Medical Informatics 47 (1997) 193–214 SUTIL: Intelligent ischemia monitoring system J. Vila a ... Cited by 13 - View as HTML - Web Search - BL Direct

Mikael Laurson,\* Cumhur Erkut - group of 5 »

V Välimäki, M Kuuskankare - Computer Music Journal, 2001 - MIT Press ... Database of excitation **signals Database** of damping signals Figure 2. Block diagram of the guitar string model. ... The **design** prevents high deviations of the ... Web Search

Professor J. Hullett Head of School School of Electrical and Computer Engineering - group of 2 »

K Street - 1999 - thesis.ece.curtin.edu.au

... Development of the system included the **design** and implementation of a hardware interface board and its control software. ... the **design** of the hardware interface. ... View as HTML - Web Search

[PS] Integrating Interactive Tools using Concurrent Haskell and Synchronous Events

EW Karlsen - CLaPF'97: 2nd Latin-American Conference on Functional ..., 1997 - informatik.uni-bremen.de

Page 1. - 1 - Integrating Interactive Tools using Concurrent Haskell and

Synchronous Events Einar W. Karlsen Universität Bremen ...

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'signal database"

1970

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## The translational termination signal database (TransTerm) now also includes initiation contexts - group of 8 »

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CM Brown, PA Stockwell, ME Dalphin, WP Tate - Nucleic Acids Res, 1994 - pubmedcentral.nih.gov ... The translational termination signal database (TransTerm) now also includes

initiation contexts. ... The translational termination signal database. ...

Cited by 36 - Web Search - BL Direct

# SIGNAL SCAN 4. 0: additional databases and sequence formats - group of 4 »

DS Prestridge - Bioinformatics, 1996 - bioinformatics.oxfordjournals.org

... Prestridge, 1991). The signal database was originally developed from transcription

factor binding sites reported in the literature. However ...

Cited by 38 - Web Search - BL Direct

## Decoding with the A: I wobble pair is inefficient - group of 4 »

JF Curran - Nucleic Acids Res, 1995 - pubmedcentral.nih.gov

... The translational termination signal database (TransTerm) now also includes

initiation contexts. ... The translational termination signal database. ...

Cited by 28 - Web Search - BL Direct

## The Cricket location-support system - group of 67 »

NB Priyantha, A Chakraborty, H Balakrishnan - Proceedings of the 6th annual international conference on ..., 2000 portal.acm.org

Page 1. The Cricket Location-Support System Nissanka B. Priyantha, Anit

Chakraborty, and Hari Balakrishnan MIT Laboratory for Computer ...

Cited by 762 - Web Search

#### Feature representations for monitoring of tool wear - group of 4 »

SB Narayanan, J Fang, G Bernard, L Atlas - Acoustics, Speech, and Signal Processing, 1994. ICASSP-94., ..., 1994 ieeexplore.ieee.org

... tools to identify, extract and process Lhese non-stationary features, and c) stress

the need for a fully annotated public-domain manufacturing signal database. ...

Cited by 8 - Web Search - BL Direct

#### The European Bioinformatics Institute (EBI) databases - group of 4 »

DB Emmert, PJ Stoehr, G Stoesser, GN Cameron - Nucleic Acids Res, 1994 - pubmedcentral nih gov

... 3020. [ Free Full text in PMC]; Brown CM, Dalphin ME, Stockwell PA, Tate

WP. The translational termination signal database. Nucleic ...

Cited by 37 - Web Search - BL Direct

#### A new cardiovascular signal database for assessing methods for analysis of ischemic heart disease

A Taddei, M Emdin, M Varanini, G Nassi, M ... - Computers in Cardiology 1996, 1996 - jeeexplore.jeee.org

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of Ischemic Heart Disease A Taddei, M Emdin, M Varanini ...

Cited by 2 - Web Search - BL Direct

#### Volcano Communications Concept - group of 2 »

A Rajnak, K Tindell, L Casparsson - Volcano Communication Technologies AB, 1998 - volcanoautomotive.com

... tools. Page 6. The VOLCANO Communications Concept page 6 (11) © VCT AB

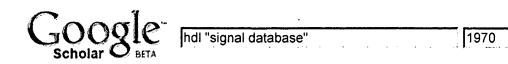
1998 5 The Signal Database And Frame Compiler The Volcano ...

Cited by 6 - View as HTML - Web Search - Library Search

#### A respiration-related EKG database - group of 2 »

F Pinciroli, G Pozzi, P Rossi, M Piovosi, A Capo, ... - Computers in Cardiology 1988. Proceedings., 1988 - ieeexplore.ieee.org ... This paper reports on the construction of an ERG—and— respiratory signal database.

The database consists of 20 recordings of some 25 minutes. ...



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Department of Electrical and Computer Engineering - group of 3 »

JB Knorr, M Tummals - 2000 - nps.edu

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An Experiment with the LOTOS Formal Description Technique on the Flight Warning Computer of Airbus ... - group of 3 »

H GARAVEL, RP HAUTBOIS - Proceedings of First AMAST International Workshop on Real- ..., 1993 - inrialpes.fr ... de Grenoble), UJF (Universite Joseph Fourier, Grenoble-I) and **VERILOG** SA. ... be formalized easily: ("The FWC is parametrized with a **signal database** and must be ... Cited by 1 - View as HTML - Web Search

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#### A VHDL reuse workbench - group of 2 »

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G Lehmann, B Wunder, KD Muller-Glaser - Design Automation Conference, 1996, with EURO-

VHDL'96 and ..., 1996 - ieeexplore.ieee.org

... very detailed queries (eg concerning signal initialization), we must store the VHDL models in a fine-grained manner. More- over, the database model should not ... Cited by 12 - Web Search

## [воок] Program Slicing of Hardware Description Languages - group of 11 »

EM Clarke... - 1999 - Springer

... Since the two cases of the theorem are captured using the master process and our notion of signal dependence, any inter-process ... VHDL Program CFGS Database ... Cited by 40 - Web Search - Library Search - BL Direct

#### Using Ada as an HDL - group of 2 »

S Ghosh - Design & Test of Computers, IEEE, 1988 - ieeexplore.ieee.org ... Actual Circuit Ada Model Component type Task type Component instance Task instance Signal path Message Connectivity Interconnection database N input terminals ... Cited by 2 - Web Search

## Creating a C++ library for Transaction-Based Test Bench Authoring - group of 3 »

S Cox, M Glasser, W Grundmann, CN Ip, W Paulsen, ... - Forum in Design Languages, 2001 - testbuilder-jp.com ... adaptor stores information such as variable values and transactions into a database of your ... user does not need to provide the full path of HDL signal a, when ... Cited by 1 - View as HTML - Web Search

#### Design of mixed-signal systems-on-a-chip - group of 8 »

K Kundert, H Chang, D Jefferies, G Lamant, E ... - Computer-Aided Design of Integrated Circuits and Systems, ..., 2000 ieeexplore.ieee.org

... suchatooliswellintegratedwithalltheotherapplications: • using a common database; • using a ... as Verilog and VHDL have been ... placement in mixed signal systems. ... Cited by 45 - Web Search - BL Direct

#### VHDL **signal** analysis in VALET - group of 3 »

C Costi, DM Miller - Communications, Computers and Signal Processing, 1999 IEEE ..., 1999 - ieeexplore ieee.org ... be pro- vided within the reusable module database. ... description; (iii) input and output signal width are ... components described in the VHDL hardware description ... Web Search

#### Using XML for Representation and Visualization of Elaborated VHDL-AMS Models - group of 4 »

T Karayiannis, J Mades, T Schneider, A Windisch, W ... - VHDL International Users Forum Fall Workshop, 2000. ..., 2000 doi.ieeecomputersociety.org

... Since each class in the database is uniquely named ... Hierarchical VHDL-AMS Models for Mixed-Signal Simulation ... Proceedings of the Inter- national HDL Conference and ... Web Search

#### ATPRG: an automatic test program generator using HDL-A for fault diagnosis of analog/mixed-signal ...

WH Huang, CL Wey - Instrumentation and Measurement, IEEE Transactions on, 1998 - ieeexplore ieee.org ... Once the database is built successfully, the routine, test ... and CL Wey, "Development of HDL-A modeled ... fault diagnosis of analog/mixed-signal circuits," IN ... Web Search - BL Direct

# <u>Computer-aided design of analog and mixed-signal integratedcircuits - group of 2 »</u>

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